Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-3. (Cancelled)

4. (Previously Presented) A data processor comprising:

a random access memory;

a processing unit for carrying out data processing while accessing said random access memory;

a first retain circuit for storing previous data output by said processing unit; and

a subtracter for taking a difference between the previous data stored in said retain circuit and current data output by said processing unit when said processing unit writes data into said random access memory.

5. (Previously Presented) The data processor according to claim 4, further comprising a variable-length coder for applying variable-length coding on difference data output from said subtracter for output to said random access memory.

6. (Previously Presented) The data processor according to claim 4, further comprising:

a first detection circuit for detecting a data write timing of a predetermined period including the write timing of the first data out of the data write timing into said random access memory by said processing unit; and

a first selector for selecting data output from said processing unit at the timing detected by said first detection circuit for output, and selecting difference data output from said subtracter at a timing other than the timing detected by said first detection circuit for output.

7. (Previously Presented) The data processor according to claim 4, further comprising:

a second retain circuit for storing previous data output to said processing unit; and

an adder for adding difference data output from said random access memory to said previous data stored in said second retain circuit.

8. (Previously Presented) The data processor according to claim 7, further comprising a variable-length decoder for applying variable-length decoding on variable-length coded difference data output from said random access memory to output the decoded data to said adder.

9. (Previously Presented) The data processor according to claim 7, further comprising:

a second detection circuit for detecting a data readout timing of a predetermined period including the readout timing of the first data among the data readout timing by said processing unit; and

a second selector for selecting data output from said random access memory at the timing detected by said second detection circuit for output, and selecting the data output from said adder at a timing other than said timing detected by said second detection circuit for output.

10-12. (Cancelled)